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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/240,975	01/29/99	MITSUISHI N	HIT-2-010-1-

TM02/0131

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EXAMINER	
BRAGDON, R	
ART UNIT	**PAPER NUMBER**
2185	11

DATE MAILED: 01/31/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/240,975	Mitsuishi
Examiner	**Group Art Unit**
Reginald Bragdon	2185

☒ Responsive to communication(s) filed on *Nov 20, 2000*

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *21-30* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *21-30* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 21-30 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21-22, 24-25, and 27-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Ugon (4,382,279).

As per claims 21, 24, and 28-30, Ugon teaches a microprocessor architecture including an EPROM 101 (see figure 2, section M2, and column 6, lines 10-11), a ROM section ("a memory"; see figure 2, section M1, and column 6, lines 5-8), and a processing and control unit 104 ("CPU"; see figures 1-2). Evolving or modifiable data or instructions, including a processing program, are stored in the section M2 ("an [EPROM] which has a first region to store a user program...and a second region to store data", where individual addresses within the M2 section represent "regions"; see column 5, lines 24-26 and column 6, lines 4-5). The section M1 contains a subprogram "PROG" ("write control program" or "second program") which performs the functions required for writing to the memory. See column 6, lines 63-66. The M1 and M2 sections are inherently located at mutually different address positions.

A main program running includes an instruction, CALL PROG, which calls or jumps to the PROG subroutine. See column 7, lines 55-65. The subroutine includes a return instruction, RET, which causes the subroutine to be exited and control returned to the main program. See column 7, lines 34-54, in particular line 54.

Furthermore, Ugon teaches a bus D which provides addresses to address registers A1 102 and A2 103 as well as data to data register D 106. Although Ugon does not specify whether this bus is comprised of physically separate address and data busses or a multiplexed address/data bus, Applicant appears to be assuming that the bus is a multiplexed address/data bus. However, a multiplexed address/data bus would meet the claim limitations since at one point in time the bus is dedicated to providing address data to the address registers A1 102 and/or A2 103 and at another time dedicated to providing data to data register D 106. Therefore, Ugon teaches "a data bus" and "an address bus".

As per claims 22 and 25, Ugon teaches that the subroutine "PROG" is located in ROM memory. See column 6, lines 5-8 and 63-66.

As per claims 27, Ugon teaches that subroutine "PROG" performs the functions required for writing to the memory. See column 6, lines 63-66.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ugon.

Ugon does not teach that the "memory" set forth as section M1 is a random access memory (RAM) or that the subroutine "PROG" is copied to the RAM for execution. It would have been obvious to one of ordinary skill in the art to have replaced the memory set forth as section M1 with a RAM and to copy the subroutine "PROG" from the EPROM to the RAM because removing the ROM would reduce the cost of manufacture by having to create only one memory (i.e. EPROM) storing the running program and the subroutine instead of two memories (i.e. EPROM and ROM) each storing different programs while utilizing the RAM (as a "shadow memory") would provide fast access to the subroutine program when modifying the EPROM.

Response to Arguments

6. Applicant's arguments filed 11-20-2000 have been fully considered but they are not persuasive.

Applicant argues that the evolving or instructions including a processing program are not stored in section M2 (see page 7 of the response). However, Ugon clearly teaches at column 6, lines 4-5 that "block M2 contains the evolving programs or parts of programs". Therefore, every application (including "user" or "first" programs as claimed) that contains evolving programs or program parts is stored in block M2 (noting the Ugon further teaches that "the majority of

applications" can be constructed with block M1 containing non-evolving programs or parts of programs and M2 containing evolving programs or parts of programs. See column 6, lines 1-5).

Applicant also argues that the "common bus structure" set forth in the present invention results in "one address space". However, the structure of the bus, whether it be separate address/data busses or a multiplexed data/address bus, does not dictate whether the memories are or are not contained within "one address space". Furthermore, the fact that Ugon teaches that "majority of applications" are constructed in such a way that memory block M1 contains all the non-evolving programs or parts of programs and M2 containing evolving programs or parts of programs (see column 6, lines 1-5) indicates that the blocks M1 and M2 must be within "one address space" since in order for the application to be run with "program parts" in different memories, then the operating system must have a unified address space for control of the application.

The Examiner notes that the newly added claim limitation have been addressed above in the rejection under 35 U.S.C. 102(b), with the assumption that Ugon teaches a multiplexed data/address bus. It goes without saying that if Ugon teaches physically dedicated and separate address and data busses, then Ugon also teaches the claim limitations. Applicant should note that is the claims are amended to recite physically dedicated and separate address and data busses (with the assumption that Ugon teaches a multiplexed address/data bus), then a rejection of the claims under 35 U.S.C. 103 would be appropriate since the use of separate address and data busses results in faster bus transfers since multiplexing between an address and data bus is not

required. However, regardless of the address/data bus structure claimed, the bus structure does not affect the "mutually different addresses in one address space" as asserted by Applicant.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. **Any response to this final action should be mailed to:**

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 305-9051, (for formal communications; please mark "EXPEDITED PROCEDURE")

Or:

(703) 305-9731 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2185

RGB
January 29, 2001